Impact of Channel Length Reduction and Doping Variation on Multigate FinFETs

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***Abstract*— In this paper we report simulation results of various multigate FinFET (MugFET) structures using SILVACO TCAD software. We simulate Tri gate, Pi gate, Omega gate and Gate all around (GAA) device structures with varied gate length and doping density and also obtain some of their electrical parameters via simulation. We show that variation in gate length and doping concentration directly affect the key electrical parameters of FinFET structures. The change in current voltage characteristics due to scaling of these devices down to nanometer range (from 16 nm to 4 nm) have been investigated with associated short channel effects (SCE). We have found results that are expected from physics- reduced on current, increased DIBL, increased subthreshold swing, lower on/off ratio etc. Our investigation aims to propose GAA as the best FinFET candidate among discussed MugFETs in sub 16 nm technology on basis of SCE handling criteria.**

Keywords—: device scaling, multigate FinFETS, short channel effects, subthreshold swing, DIBL, high-k dielctric

I. INTRODUCTION

For last few decades CMOS technology is undergoing drastic reduction in device size to maintain the miniaturization trend. Objective of this trend is integrating more electrical components in per unit bound area with improved performance at less expense. Remarkably followed by "Moore's law", continuous downscaling of MOSFET devices has led us to a very challenging era of modeling semiconductor physics.

As the device size gradually shrinks, serious contest occurs between gate length and device performance and thus different Short Channel Effects (SCE) are introduced [1]. When the channel length and the depletion layer width are of same order of magnitude, it's called "Short Channel". As a result, a variety of problems like– Threshold Voltage Roll-Off (TVRO), subthreshold conduction, Drain Induced Barrier Lowering (DIBL), reduced on current, smaller On/Off ratio etc. related to device performance have then emerged [2]. In classical CMOS technology, improvement in compact model designing also deals with crucial challenges like- speed of the device and power consumption [3].

In this paper, multigate structure with the advantage of having multiple gates, is assumed the solution of SCE drawbacks in device performance. Multi-gate transistors (FETs) with three-dimensional (3D) channel is becoming promising candidates to overcome the scaling issues of planar FETs because of their excellent SCE immunity due to better electrostatic control of the channel potential by gate electrodes wrapped on multiple sides [4]. FinFET, having a thin fin shaped body, is found as the best candidate among nonplanar devices for future nanoscale CMOS technologies. Actually thin vertical channel is defined as "Fin" and this channel can be controlled by multiple gates surrounding the fin body. Among the most feasible candidates of multigate FinFET we choose Tri gate, Pi gate, Omega Gate and Gate All Around (GAA) structures for our investigation.

A 3D non planar FinFET where the hard mask at top of the fin is absence, having front gate control on channel from three faces including one lateral top and two vertical plane, creates a "DELTA" shape [5]. This is also called Triple (Tri-gate) gate. When the Fin allows the vertical gates to penetrate into some depth in the buried oxide (BOX), then this structure is called Pi-gate [6]. Another variant is Omega Gate (Ω) FinFET in which the gate undercuts through BOX and partially covers control on the bottom surface of the fin body [7]. When the Silicon fin is surrounded by gates from all sides with maximum possible control over channel, it is called, Gate All Around (GAA). According to the latest (2015) ITRS guideline GAA is called the "ultimate structure" [8].

In our work the assumed structure is a Silicon-On-Insulator (SOI) n-FinFET for the advantages unfolded from its buried oxide (BOX) layer because it yields improved switching speed and reduced power consumption with the reduction of parasitic capacitances [9]. High-K dielectric is used to keep the gate leakage current density to a sustainable value because scaling silicon dioxide (SiO_2) beneath 2nm and increases leakage density and decreases drain current (Ion) [10]. The channel region or the analyzed part is covered by Silicon Nitride (Si_3N_4). For several advantages compared to the doped polysilicon gate, a metal gate electrode has been used to achieve the best combination of work function and channel doping.

In our simulation the Constant Voltage and Temperature (CVT) or Lombardi model for carriers is used to capture field dependent mobility, phonon scattering limited mobility, impurity scattering limited mobility and also surface roughness induced mobility. This inversion layer model overrides any other mobility model [11]. For recombination effects of device

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Shockley Read Hall (SRH) is considered [11] which simulates the leakage current due to thermal effects and also it is useful to simulate the presence of interface trap charges. Furthermore, we chose Gummel's method (or the decoupled method), which performs Gummel iteration for the Newton solution [11].

Our study includes the impact of varied gate length and varied doping concentration on significant device parameters such as-threshold voltage (Vth), drain induced barrier lowering (DIBL), subthreshold swing (SS), on current (I_{on}), leakage current (I_{off}), on/off ratio of the considered nanoscale structures.

II. Simulated 3D Device Structure

We conducted our desired simulation in SILVACO TCAD software. The parameters used in the FinFETs are estimated using SRH, CVT and Newton Gummels numerical methods.

With metal contact and strained silicon, simulated structures are observed for the gate lengths (Lg) 4, 8, 12, 16 nm. Source and drain length (L_S/L_D) is 10 nm. The vertical silicon fin height is H_{Fin}, width is W_{Fin} whereas the high-K dielectric Si_3N_4 is used with uniform oxide thickness (t_{ox}) of 1nm. Metal gate contact work function is adjusted at 4.71 eV. The channel is uniformly doped with 1.45×10^{10} cm^{-3} acceptor dopant and the source/drain region is doped with 10^{20} cm^{-3} donor concentration. Fig 1. shows the cross section view of the simulated design of 8nm Tri gate (a), Pi gate(b), Omega gate (c) and GAA (d) structures.

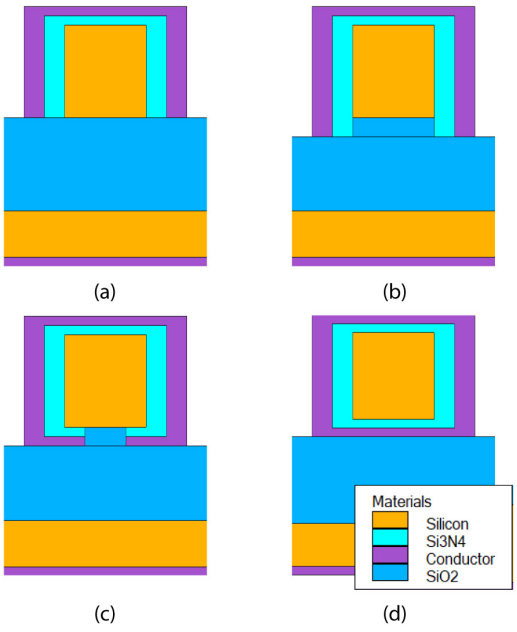

Fig. 1. Cross sectional view of (a) Tri-gate FinFET (b) Pi-gate FinFET (c) Omega-FET (d) GAA FET

TABLE I. Parameter of Multigate SOI n-FinFET Structures

Parameter	**Dimension**
L_g (nm)	4, 8, 12, 16
L_S/ L_D (nm)	10
Fin height, H_{Fin} (nm)	10
Fin width, W_{Fin} (nm)	4
Oxide thickness T_{OX} (nm)	1
Gate dielectric	Si_3N_4
Work function (eV)	4.71
N_{ch} (cm^{-3})	1.45×10^{10}
$N_{S,D}$ (cm^{-3})	10^{20}

III. Results And Discussion

Finally, from our simulation, face to face comparison among the four structures will be provided with the effect of channel length reduction and increase in channel doping concentration.

A. *Impact of Channel Length Variation*

As channel length is reduced subthreshold slope shifts from its 60mV/dec ideal value. Fig. 2 shows that for 4 nm channel length, SS is above 90 mV/dec whereas for 16 nm, it is close to the ideal value. When the device becomes shorter, the channel potential changes by the capacitances between channel and source/drain junction. Due to the increase of the minimum surface potential, the channel-source/drain capacitance will increase and accordingly the SS increases. FinFET on current I_{on} increases with decrease in gate length. As the channel length is reduced, the charge carriers experience less interface scattering. As a result an increase of the mobility causes an increased I_{on}. Also multigate structure shows improved I_{on} because of better electrostatic control. As we can see impact of

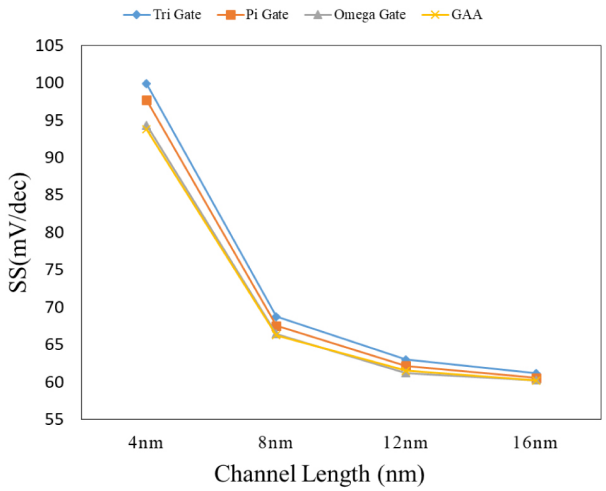

Fig. 2. Impact of Channel Length Reduction on Subthreshold Slope (SS)

channel length reduction on I_{on} in Fig. 3, GAA has better I_{on} than other structures because of lower parasitic series resistance which means an increased I_{on}.

Higher I_{on}/I_{off} represents better switching capability. But as the channel length is reduced, this ratio decreases significantly resulting in imperfect switching behavior of transistor. As we decrease the channel length, the drive current increases almost linearly, but the I_{off} increases exponentially. This leads to decrease of I_{on}/I_{off} ratio. In Fig. 4 impact of channel length reduction on I_{on}/I_{off} ratio is shown for four different structures. As the number of gate is increased, I_{on}/I_{off} ratio is further improved which is clearly seen in GAA.

B. Impact of Channel Doping Variation

Increased doping in the channel maintains the barrier between the source and drain as there are more carriers injecting into the channel being controlled by more gates even when larger drain voltage influence is present at the drain and gate junction region. So, threshold voltage is not much altered with higher drain bias and as a result DIBL is reduced. DIBL reduction with increased channel doping is estimated from the Fig. 5.

The effect of channel doping on SS is shown in Fig. 6. As the doping concentration increases SS reduces. FinFET exhibits close to ideal value of SS at doping concentration of 2×10^{19} /cm^3. A higher channel doping concentration reduces charge sharing between the gate and drain in the channel, and it creates a large potential barrier between source and drain [12]. As a result, electrostatic control of gate over the channel is increased and SS is reduced.

Fig. 7 shows effect of doping on I_{on}. From the figure it is evident that on current decreases as the channel doping is increased and it is highest for GAA. The after effect of impurity of opposite type of source/drain region is contraction

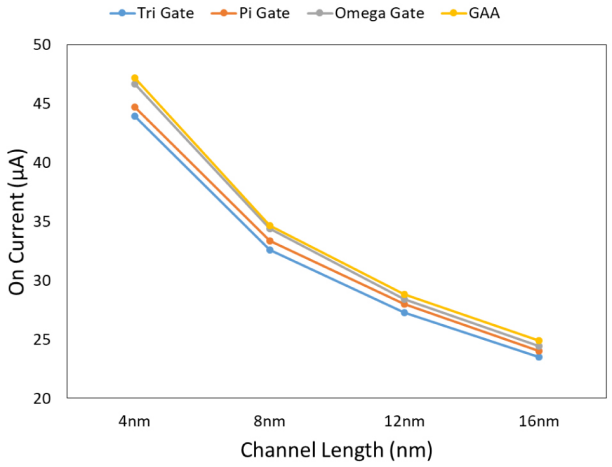

Fig. 3. Impact of Channel Length Reduction on On current.

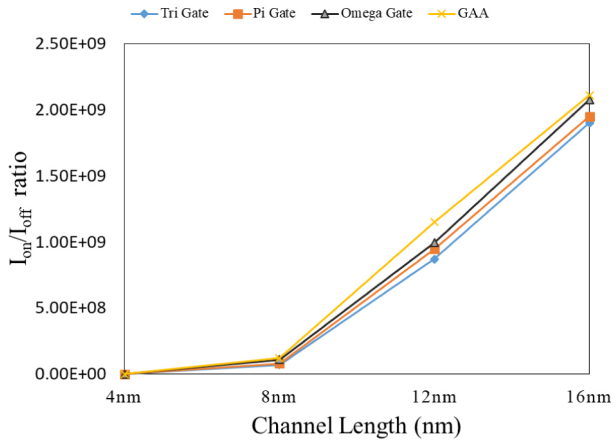

Fig. 4. Impact of Channel Length Reduction on I_{on}/I_{off} ratio.

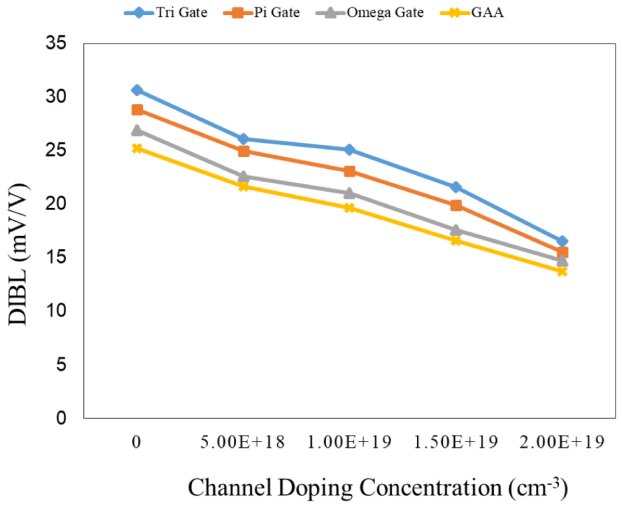

Fig. 5. Effect of Channel Doping on DIBL

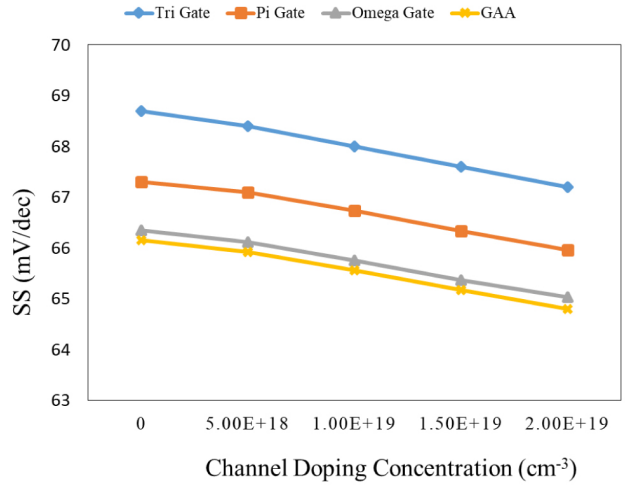

Fig. 6. Effect of Channel Doping on Subthreshold Slope (SS)

of channel length which has valuable impact on transistor conductance. The drain current is higher for lower concentration of the p-type ions in channel as DIBL reduces gradually as channel doping increases. So by increasing the channel doping of the n-FinFET device, the inversion charge density decreases which increases the threshold voltage as a result of which I_{on} decreases [12].

Fig. 8 shows the relation of channel doping concentration with FinFET I_{on}/I_{off} ratio. The ratio increases significantly with the increment of channel doping. Furthermore, Gate-all-around FinFET shows better I_{on}/I_{off} ratio than other three counterparts.

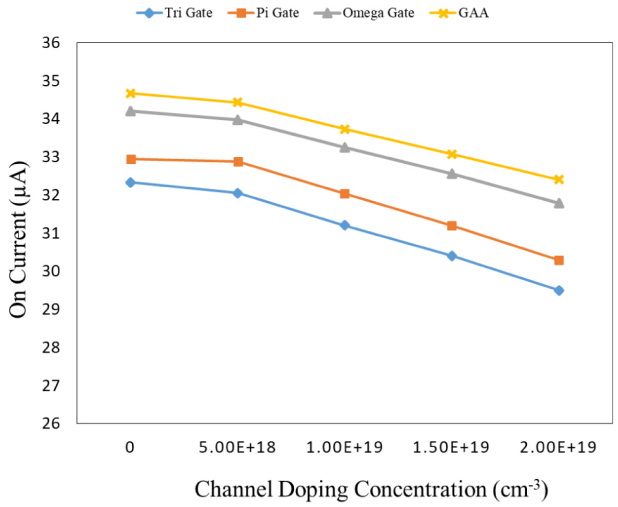

Fig. 7. Effect of Channel Doping on On current

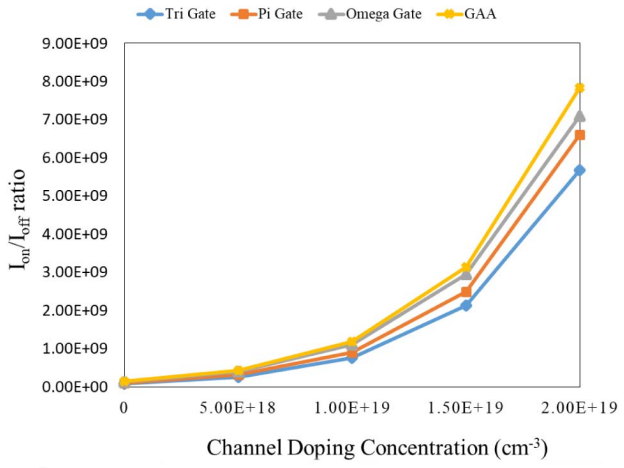

Fig. 8. Effect of Channel Doping on I_{on}/I_{off} ratio

As we increase the channel doping the drive current reduces almost linearly, but the off current decreases exponentially. This leads to an increase in I_{on}/I_{off} ratio very sharply which represents the power consumption of a device.

IV. Conclusions

Using SILVACO TCAD tool simulation and classical models for multigate n-FinFETs based on SOI we proposed four devices design those are Tri, Pi, Omega and Gate All Around considering high k dielectric and metal gate contact. The purpose of this work was to increase device performance and reduce SCEs like DIBL, leakage, Vth roll-off, etc. for reduced gate length and increased doping. Additionally we found GAA structure to have ultimate electrostatic control on threshold voltage and SCEs than Tri gate, Pi gate and Omega gate FinFET structures. GAA FinFET on SOI gives better threshold voltage.

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